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EXAMINER	
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ART UNIT	PAPER NUMBER
2666	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/036,622	RASHID ET AL.	
	Examiner	Art Unit	
	Michael J. Moore, Jr.	2666	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *39-79* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *39-79* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on 10/19/2005 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the examiner has considered the information disclosure statement.

Claim Objections

2. Claims **63-65 and 71** are objected to because of the following informalities:

Regarding claims **63-65**, claims **64 and 65** are now duplicate claims while claim **63** contains the limitations of original claim **64**. It is believed by Examiner that these claims were meant to remain in their previous state.

Regarding claim **71**, on lines 3 and 6, the word "aid" should be "said".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

Amendments made to claim **50** to overcome the rejection under 35 U.S.C. § 112 2nd paragraph of the previous Office Action are proper and have been entered. This rejection has been withdrawn.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims **39-66 and 71-79** are rejected under 35 U.S.C. 102(b) as being anticipated by Hochschild et al. (U.S. 5,805,589) ("Hochschild"). Hochschild teaches all of the limitations of the specified claims with the reasoning that follows.

Regarding claim **39**, "an apparatus" is anticipated by the switching circuit 25 shown in Figure 3A.

"A set of input ports" is anticipated by input ports 310 within switching circuit 25 (apparatus) of Figure 3A.

"A FIFO storage buffer" is anticipated by central queue 350 (FIFO storage buffer) within switching circuit 25 (apparatus) of Figure 3A.

"Request logic coupling the set of input ports to the FIFO storage buffer" is anticipated by central queue input LRU arbiter 385 (request logic) of Figure 3B that couples input ports 310 to central queue 350 via input request and grant signals.

"A memory in communication with the request logic, wherein the memory concurrently maintains a plurality of pointers, wherein each pointer in the plurality of pointers corresponds to a different location in the FIFO storage buffer for storing data from an input port in the set of input ports" is anticipated by message pointer RAM 720 (memory) within central queue 350 of Figure 8 that contains a plurality of pointers that each point to a location in chunk storage RAM 715 as shown in Figure 7 and spoken of on column 23, lines 28-48.

Lastly, "wherein the request logic simultaneously writes data to the FIFO storage buffer for at least two of the input ports" is anticipated by central queue input LRU arbiter 385 (request logic) of Figure 3B that receives central queue input request signals

from input ports 310 of Figure 3A and issues a write enable signal to central queue 350 so that 64-bit incoming data chunks are then written to chunk storage RAM 715 as shown in Figure 8.

Regarding claim **40**, "a first entry that maintains a pointer corresponding to a first location in the FIFO storage buffer for storing a first set of data from an input port in the set of input ports" as well as "a second entry that maintains a pointer corresponding to a second location in the FIFO storage buffer for storing a second set of data from an input port in the set of input ports" is anticipated by the 128 7-bit locations shown in message pointer RAM 720 of Figure 7 that each indicate a location of data in chunk storage RAM 715 as spoken of on column 23, lines 28-37.

Regarding claim **41**, "a third entry that maintains a pointer corresponding to a third location in the FIFO storage buffer for storing a third set of data from an input port in the set of input ports" as well as "a fourth entry that maintains a pointer corresponding to a fourth location in the FIFO storage buffer for storing a fourth set of data from an input port in the set of input ports" is anticipated by the 128 7-bit locations shown in message pointer RAM 720 of Figure 7 that each indicate a location of data in chunk storage RAM 715 as spoken of on column 23, lines 28-37.

Regarding claim **42**, "wherein the memory maintains a data identifier for each pointer in the plurality of pointers" is anticipated by the 128 7-bit locations shown in message pointer RAM 720 of Figure 7 that each indicate a location of data in chunk storage RAM 715 as spoken of on column 23, lines 28-37.

Regarding claim **43**, "wherein each data identifier identifies a data source" is anticipated by the 128 7-bit locations shown in message pointer RAM 720 of Figure 7 that each indicate a location of data in chunk storage RAM 715 as spoken of on column 23, lines 28-37.

Regarding claim **44**, "wherein the memory is a content addressable memory" is anticipated by message pointer RAM 720 of Figure 7.

Regarding claim **45**, "wherein the request logic and the storage buffer are included in a multiple port memory" is anticipated by switching circuit 25 of Figure 3A that contains multiple ports 310 and 380.

Regarding claim **46**, "an apparatus" is anticipated by the switching circuit 25 shown in Figure 3A.

"A set of input ports" is anticipated by input ports 310 within switching circuit 25 (apparatus) of Figure 3A.

"A FIFO storage buffer" is anticipated by central queue 350 (FIFO storage buffer) within switching circuit 25 (apparatus) of Figure 3A.

"Request logic coupling the set of input ports to the FIFO storage buffer" is anticipated by central queue input LRU arbiter 385 (request logic) of Figure 3B that couples input ports 310 to central queue 350 via input request and grant signals.

"Wherein the request logic simultaneously writes data to the FIFO storage buffer for at least two of the input ports" is anticipated by central queue input LRU arbiter 385 (request logic) of Figure 3B that receives central queue input request signals from input ports 310 of Figure 3A and issues a write enable signal to central queue 350 so that 64-

bit incoming data chunks are then written to chunk storage RAM 715 as shown in Figure 8.

"A memory in communication with the request logic, wherein the memory concurrently maintains a plurality of pointers, wherein each pointer in the plurality of pointers corresponds to a different location in the FIFO storage buffer for storing data from an input port in the set of input ports" is anticipated by message pointer RAM 720 (memory) within central queue 350 of Figure 8 that contains a plurality of pointers that each point to a location in chunk storage RAM 715 as shown in Figure 7 and spoken of on column 23, lines 28-48.

"Wherein the memory maintains a data identifier for each pointer in the plurality of pointers, wherein each data identifier identifies a data source" is anticipated by the 128 7-bit locations (data identifier entry) shown in message pointer RAM 720 of Figure 7 that each indicate a location of data in chunk storage RAM 715 as spoken of on column 23, lines 28-37.

Lastly, "a first entry that maintains a pointer corresponding to a first location in the FIFO storage buffer for storing a first set of data from an input port in the set of input ports" as well as "a second entry that maintains a pointer corresponding to a second location in the FIFO storage buffer for storing a second set of data from an input port in the set of input ports" is anticipated by the 128 7-bit locations (data identifier entry) shown in message pointer RAM 720 of Figure 7 that each indicate a location of data in chunk storage RAM 715 as spoken of on column 23, lines 28-37.

Regarding claim **47**, "a third entry that maintains a pointer corresponding to a third location in the FIFO storage buffer for storing a third set of data from an input port in the set of input ports" as well as "a fourth entry that maintains a pointer corresponding to a fourth location in the FIFO storage buffer for storing a fourth set of data from an input port in the set of input ports" is anticipated by the 128 7-bit locations shown in message pointer RAM 720 of Figure 7 that each indicate a location of data in chunk storage RAM 715 as spoken of on column 23, lines 28-37.

Regarding claim **48**, "wherein the memory is a content addressable memory" is anticipated by message pointer RAM 720 of Figure 7.

Regarding claim **49**, "wherein the request logic and the storage buffer are included in a multiple port memory" is anticipated by switching circuit 25 of Figure 3A that contains multiple ports 310 and 380.

Regarding claim **50**, "a sink port" is anticipated by the switching circuit 25 shown in Figure 3A.

"A multiple entry point FIFO having a plurality of data inputs in communication with a set of input ports to accept and store data" is anticipated by central queue 350 (multiple entry point FIFO) that receives a plurality of input data from input ports 310 as shown in Figure 3A as well as Figure 8.

"An output port coupled to the multiple entry point FIFO to receive the data from the multiple entry point FIFO and transmit the data on a communications link" is anticipated by output ports 380 shown in Figure 3A that receive output data from central queue 350 and output data on leads 390.

Regarding claim **51**, "a FIFO storage buffer" is anticipated by chunk storage RAM 715 within central queue 350 (multiple entry point FIFO) of Figure 8.

"Request logic coupling the plurality of data inputs to the FIFO storage buffer" is anticipated by control circuitry 830 (request logic) coupled to data input from input ports 310 via chunk storage RAM 715 as shown in Figure 8.

Lastly, "a memory in communication with the request logic, wherein the memory concurrently maintains a plurality of pointers, wherein each pointer in the plurality of pointers corresponds to a different location in the FIFO storage buffer for storing data from an input port in the set of input ports" is anticipated by message pointer RAM 720 (memory) within central queue 350 of Figure 8 that contains a plurality of pointers that each point to a location in chunk storage RAM 715 as shown in Figure 7 and spoken of on column 23, lines 28-48.

Regarding claim **52**, "a first entry that maintains a pointer corresponding to a first location in the FIFO storage buffer for storing a first set of data from an input port in the set of input ports" as well as "a second entry that maintains a pointer corresponding to a second location in the FIFO storage buffer for storing a second set of data from an input port in the set of input ports" is anticipated by the 128 7-bit locations shown in message pointer RAM 720 of Figure 7 that each indicate a location of data in chunk storage RAM 715 as spoken of on column 23, lines 28-37.

Regarding claim **53**, "a third entry that maintains a pointer corresponding to a third location in the FIFO storage buffer for storing a third set of data from an input port in the set of input ports" as well as "a fourth entry that maintains a pointer corresponding

to a fourth location in the FIFO storage buffer for storing a fourth set of data from an input port in the set of input ports" is anticipated by the 128 7-bit locations shown in message pointer RAM 720 of Figure 7 that each indicate a location of data in chunk storage RAM 715 as spoken of on column 23, lines 28-37.

Regarding claim **54**, "wherein the memory maintains a data identifier for each pointer in the plurality of pointers" is anticipated by the 128 7-bit locations shown in message pointer RAM 720 of Figure 7 that each indicate a location of data in chunk storage RAM 715 as spoken of on column 23, lines 28-37.

Regarding claim **55**, "wherein each data identifier identifies a data source" is anticipated by the 128 7-bit locations shown in message pointer RAM 720 of Figure 7 that each indicate a location of data in chunk storage RAM 715 as spoken of on column 23, lines 28-37.

Regarding claim **56**, "wherein the memory is a content addressable memory" is anticipated by message pointer RAM 720 of Figure 7.

Regarding claim **57**, "wherein the request logic and the storage buffer are included in a multiple port memory" is anticipated by switching circuit 25 of Figure 3A that contains multiple ports 310 and 380.

Regarding claim **58**, "a cross-bar switch" is anticipated by the switching circuit 25 shown in Figure 3A.

"A set of input ports to receive data packets" is anticipated by input ports 310 within switching circuit 25 of Figure 3A.

"A set of sink ports in communication with the set of input ports to accept and forward the data packets" is anticipated by output ports 380 of Figure 3A that receive data from input ports 310 via central queue 350.

Lastly, "wherein a first sink port in the set of sink ports includes a multiple entry point FIFO having a plurality of data inputs that store data from data packets accepted by the first sink port" is anticipated by the FIFO 620 (multiple entry point FIFO) within output port 380 of Figure 6 that receives a plurality of input data via multiple input lines.

Regarding claim **59**, "a FIFO storage buffer" is anticipated by chunk storage RAM 715 within central queue 350 of Figure 8.

"Request logic coupling the plurality of data inputs to the FIFO storage buffer" is anticipated by control circuitry 830 (request logic) coupled to data input from input ports 310 via chunk storage RAM 715 as shown in Figure 8.

Lastly, "a memory in communication with the request logic, wherein the memory concurrently maintains a plurality of pointers, wherein each pointer in the plurality of pointers corresponds to a different location in the FIFO storage buffer for storing data from an input port in the set of input ports" is anticipated by message pointer RAM 720 (memory) within central queue 350 of Figure 8 that contains a plurality of pointers that each point to a location in chunk storage RAM 715 as shown in Figure 7 and spoken of on column 23, lines 28-48.

Regarding claim **60**, "a first entry that maintains a pointer corresponding to a first location in the FIFO storage buffer for storing a first set of data from an input port in the set of input ports" as well as "a second entry that maintains a pointer corresponding to a

second location in the FIFO storage buffer for storing a second set of data from an input port in the set of input ports" is anticipated by the 128 7-bit locations shown in message pointer RAM 720 of Figure 7 that each indicate a location of data in chunk storage RAM 715 as spoken of on column 23, lines 28-37.

Regarding claim **61**, "a third entry that maintains a pointer corresponding to a third location in the FIFO storage buffer for storing a third set of data from an input port in the set of input ports" as well as "a fourth entry that maintains a pointer corresponding to a fourth location in the FIFO storage buffer for storing a fourth set of data from an input port in the set of input ports" is anticipated by the 128 7-bit locations shown in message pointer RAM 720 of Figure 7 that each indicate a location of data in chunk storage RAM 715 as spoken of on column 23, lines 28-37.

Regarding claim **62**, "wherein the memory maintains a data identifier for each pointer in the plurality of pointers" is anticipated by the 128 7-bit locations shown in message pointer RAM 720 of Figure 7 that each indicate a location of data in chunk storage RAM 715 as spoken of on column 23, lines 28-37.

Regarding claim **63**, "wherein the memory is a content addressable memory" is anticipated by message pointer RAM 720 of Figure 7.

Regarding claims **64 and 65**, "wherein the request logic and the storage buffer are included in a multiple port memory" is anticipated by switching circuit 25 of Figure 3A that contains multiple ports 310 and 380.

Regarding claim **66**, "wherein each sink port in the set of sink ports includes a multiple entry point FIFO having a plurality of data inputs" is anticipated by output ports 380 of Figure 3A that each contain a FIFO 620 as shown in Figure 6.

Regarding claim **71**, "accepting data from a first data packet, wherein the data accepted is a subset of the first data packet, storing the data from the first data packet in a FIFO, accepting data from a second data packet, wherein the data accepted is a subset of the second data packet, and storing the data from the second data packet in the FIFO" is anticipated by the chunks of data received from input ports 310 of Figure 3A and stored in chunk storage RAM 715 (FIFO) that are associated with different messages (data packets) as spoken of on column 23, lines 28-48.

Regarding claim **72**, "wherein the first data packet originates from a first source and the second data packet originated from a second source" is anticipated by the chunks of data received from input ports 310 (different sources) of Figure 3A and stored in chunk storage RAM 715 (FIFO) that are associated with different messages (data packets) as spoken of on column 23, lines 28-48.

Regarding claim **73**, "determining that the first data accepted includes a first line of the first data packet, allocating a first location in the FIFO for storing data from the first data packet, determining that the second data accepted includes a first line of the second data packet, and allocating a second location in the FIFO for storing data from the second data packet" is anticipated by the chunks of data received from input ports 310 (different sources) of Figure 3A and stored in chunk storage RAM 715 (FIFO) that

are associated with different messages (data packets) as spoken of on column 23, lines 28-48.

Regarding claim **74**, "creating a first pointer to the first location" is anticipated by the stored pointers in message pointer RAM 720 of Figure 7 that indicate location of message chunks in chunk storage RAM 715.

Lastly, "creating a first tag identifying the first data packet" is anticipated by the address information stored in registers 730 that point to the location pointers of message pointer RAM 720 indicating a corresponding output port for each message.

Regarding claim **75**, "creating a second pointer to the second location" is anticipated by the stored pointers in message pointer RAM 720 of Figure 7 that indicate location of message chunks in chunk storage RAM 715.

Lastly, "creating a second tag identifying the second data packet" is anticipated by the address information stored in registers 730 that point to the location pointers of message pointer RAM 720 indicating a corresponding output port for each message.

Regarding claim **76**, "wherein the first tag identifies a source of the first data packet and the second tag identifies a source of the second data packet" is anticipated by the address information stored in registers 730 that point to the location pointers of message pointer RAM 720 indicating a corresponding output port for each message sent from a corresponding input port.

Regarding claim **77**, "accepting additional data for the first data packet, determining the additional data accepted does not include a first line of the first data packet, identifying a position in the first location in the FIFO for storing the additional

data from the first data packet, accepting additional data fro the second data packet, determining that the additional data accepted does not include a first line of the second data packet, and identifying a position in the second location in the FIFO for storing the additional data from the second data packet is anticipated by the chunks of data received from input ports 310 of Figure 3A and stored in chunk storage RAM 715 (FIFO) that are associated with different messages (data packets) as spoken of on column 23, lines 28-48.

Regarding claim **78**, "retrieving a pointer to the position in the first location, and retrieving a pointer to the position in the second location" is anticipated by the stored pointers in message pointer RAM 720 of Figure 7 that indicate location of message chunks in chunk storage RAM 715.

Regarding claim **79**, "accepting additional data for the first data packet, determining that the additional data accepted includes a last line of the first data packet, purging a pointer to a position in the first location in the FIFO, accepting additional data for the second data packet, determining that the additional data accepted includes a last line of the second data packet, and purging a pointer to a position in the second location in the FIFO" is anticipated by the stored pointers in message pointer RAM 720 of Figure 7 that indicate location of message chunks in chunk storage RAM 715 as well as column 23, lines 42-48 that states that as each chunk of a particular message is transferred out of the central queue, that chunk is pulled from the head of the list with the address in corresponding location in the message pointer RAM 720 altered to point to the next chunk for that message.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims **67-70** are rejected under 35 U.S.C. 103(a) as being unpatentable over Hochschild et al. (U.S. 5,805,589) ("Hochschild") in view of Dai et al. (U.S. 6,658,016) ("Dai").

Regarding claim **67**, Hochschild teaches the switch of claim **58**. Hochschild does not teach a set of data rings in communication with the set of input ports and set of sink ports.

However, Dai teaches a packet switching fabric 10 in Figure 1 containing switching devices 12 that are coupled via a set of data rings 18 and 24.

At the time of the invention, it would have been obvious to someone of ordinary skill in the art given these references to combine the data ring teachings of Dai with the switching circuit of Hochschild in order to provide a more robust switching system with bandwidth management as spoken of on column 4, lines 49-67 of Dai.

Regarding claim **68**, Hochschild does not teach where the multiple point entry FIFO includes a data input for each data ring in the set of data rings.

However, Dai teaches a packet switching fabric 10 in Figure 1 containing switching devices 12 that are coupled via a set of data rings 18 and 24.

At the time of the invention, it would have been obvious to someone of ordinary skill in the art given these references to combine the data ring teachings of Dai with the switching circuit of Hochschild in order to provide a more robust switching system with bandwidth management as spoken of on column 4, lines 49-67 of Dai.

Regarding claim **69**, Hochschild does not teach where the first sink port snoops data packets on each data ring and determines whether to accept a first data packet based on whether the first sink port has sufficient storage space, whether the first sink port supports a destination targeted by the first data packet, and whether the total number of packets received doesn't exceed a predetermined number of packets.

However, Dai teaches a packet switching fabric 10 in Figure 1 containing switching devices 12 that are coupled via a set of data rings 18 and 24. The control ring 24 is utilized to regulate data packet transfer on the data ring 18.

At the time of the invention, it would have been obvious to someone of ordinary skill in the art given these references to combine the data ring teachings of Dai with the

switching circuit of Hochschild in order to provide a more robust switching system with bandwidth management as spoken of on column 4, lines 49-67 of Dai.

Regarding claim **70**, Hochschild does not teach a ring interface coupled to the set of data rings to accept data from a plurality of sources and supply the data on a plurality of outputs.

However, Dai teaches a packet switching fabric 10 in Figure 1 containing switching devices 12 that are coupled via a set of data rings 18 and 24 via ring ports 16 and 22.

At the time of the invention, it would have been obvious to someone of ordinary skill in the art given these references to combine the data ring teachings of Dai with the switching circuit of Hochschild in order to provide a more robust switching system with bandwidth management as spoken of on column 4, lines 49-67 of Dai.

Response to Arguments

8. Applicant's arguments with respect to claims **39-76** have been considered but are moot in view of the new ground(s) of rejection provided above.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Schwartz et al. (U.S. 6,434,115) and Han et al. (U.S. 6,633,568) are other references pertinent to this application.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael J. Moore, Jr. whose telephone number is (571)

272-3168. The examiner can normally be reached on Monday-Friday (8:30am - 5:00pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Seema S. Rao can be reached at (571) 272-3174. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Michael J. Moore, Jr.
Examiner
Art Unit 2666

mjm MM

DUNG TON
PRIMARY EXAMINER